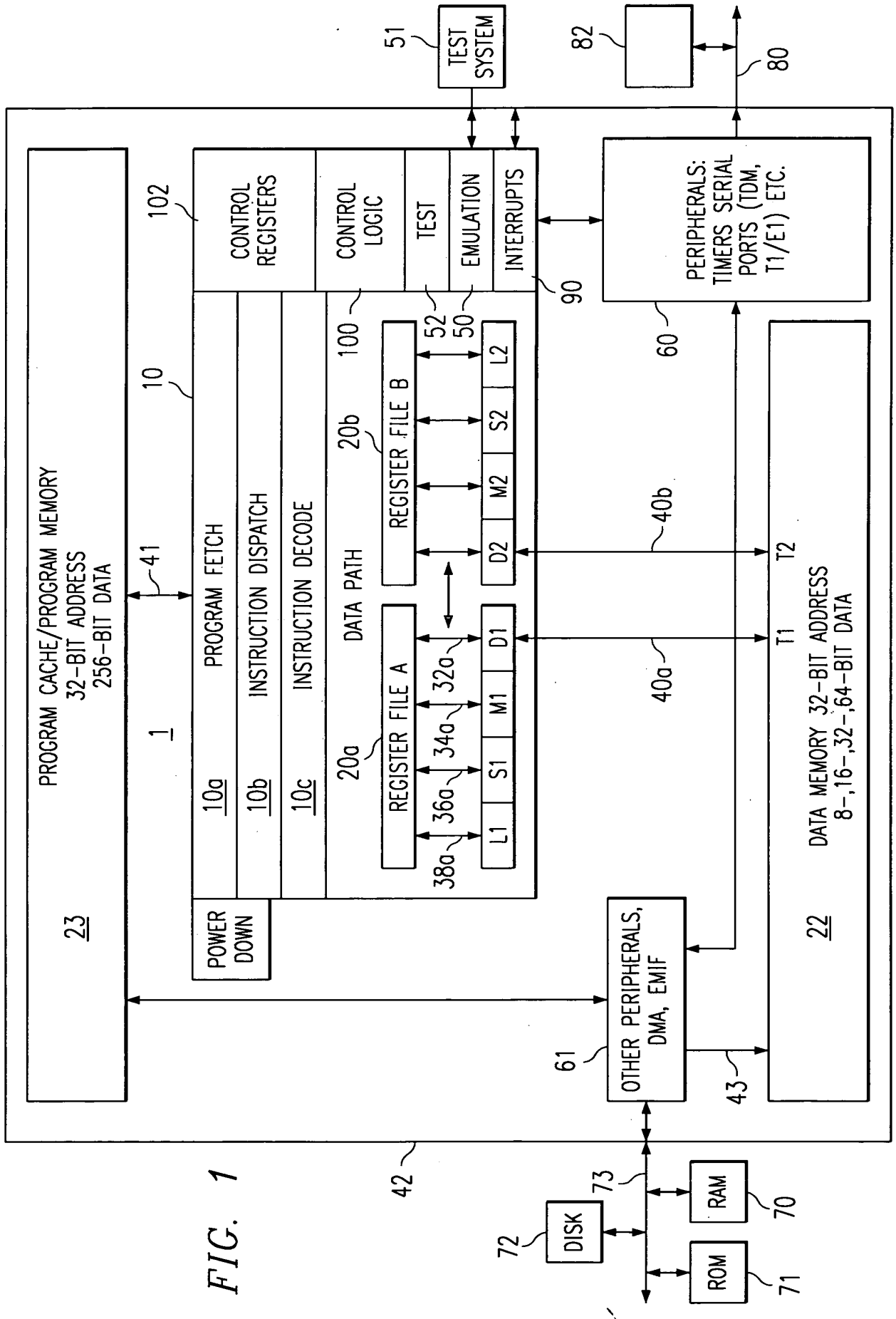

PROGRAM CACHE/PROGRAM MEMORY
32-BIT ADDRESS
256-BIT DATA
23
1
41
10
PROGRAM FETCH
INSTRUCTION DISPATCH
INSTRUCTION DECODE
DATA PATH
10a
10b
10c
20a
20b
100
REGISTER FILE A
REGISTER FILE B
L1
S1
M1
D1
D2
M2
S2
L2
32a
34a
36a
38a
50
52
CONTROL REGISTERS
CONTROL LOGIC
TEST
EMULATION
INTERRUPTS
102
90
POWER DOWN
TEST SYSTEM
51
82
80
PERIPHERALS: TIMERS SERIAL PORTS (TDM, T1/E1) ETC.
60
40a
40b
T1
T2
DATA MEMORY 32-BIT ADDRESS
8-,16-,32-,64-BIT DATA
22
OTHER PERIPHERALS, DMA, EMIF
61
43
42
73
DISK
72
RAM
70
ROM
71

FIG. 1

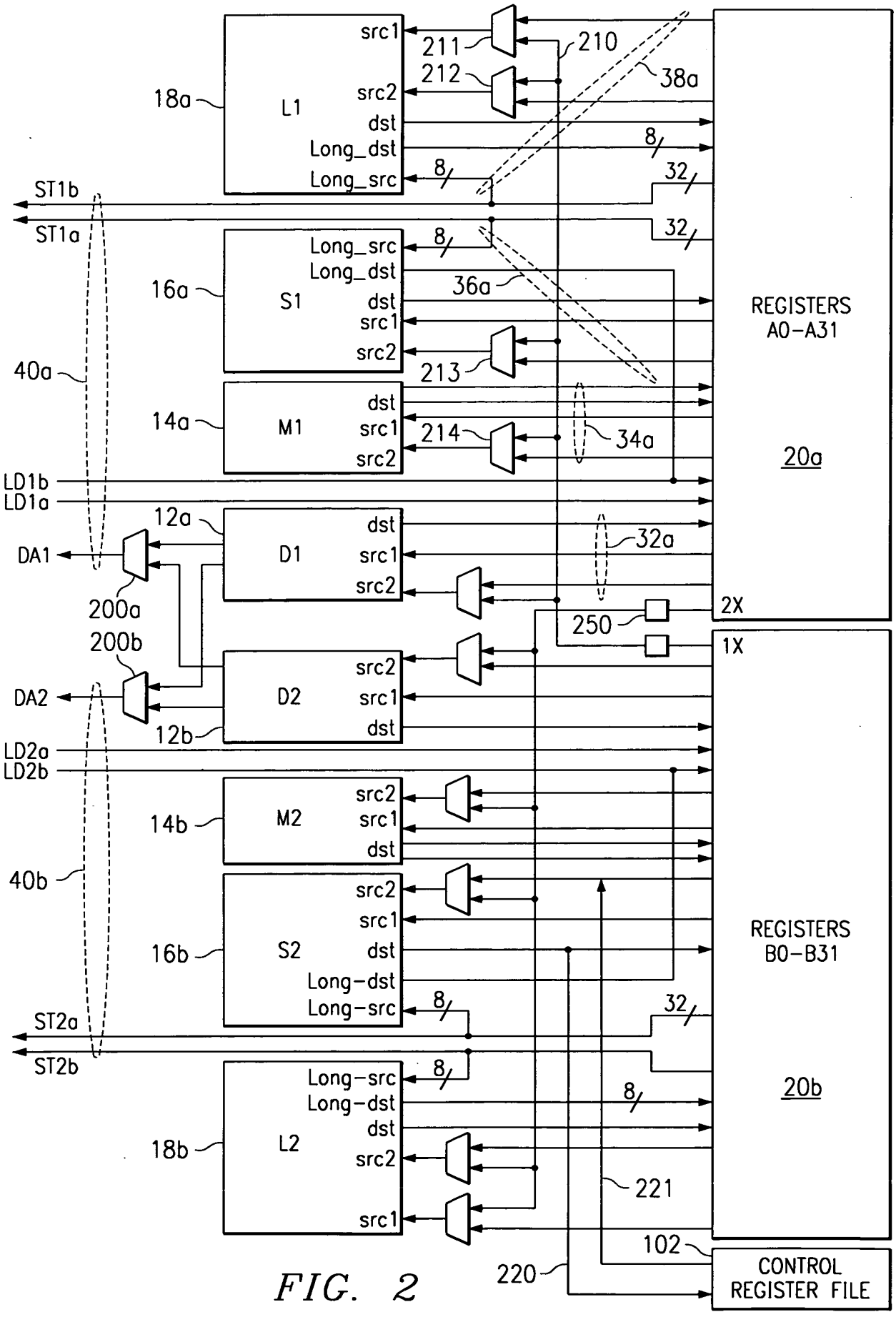

18a
L1
src1
src2
dst
Long_dst
Long_src
211
212
210
38a
8
32
ST1b
ST1a
16a
S1
Long_src
Long_dst
dst
src1
src2
36a
213
40a
14a
M1
214
34a
REGISTERS
A0-A31
20a
LD1b
LD1a
12a
D1
DA1
200a
32a
2X
250
200b
D2
DA2
12b
1X
LD2a
LD2b
14b
M2
40b
16b
S2
Long-dst
Long-src
ST2a
ST2b
18b
L2
REGISTERS
B0-B31
20b
221
102
CONTROL
REGISTER FILE
220

FIG. 2

OPERATIONS ON THE .L UNIT

31 29	28	27 23	22 18	17 13	12	11 5	4	3	2	1	0
CREG	Z	DST	SCR2	SRC1/CST	X	OP	1	1	0	S	P
3		5	5	5		7					

FIG. 3A

OPERATIONS ON THE .M UNIT

31 29	28	27 23	22 18	17 13	12	11 7	6	5	4	3	2	1	0
CREG	Z	DST	SCR2	SRC1/CST	X	OP	0	0	0	0	0	S	P
3		5	5	5		5							

FIG. 3B

OPERATIONS ON THE .D UNIT

31 29	28	27 23	22 18	17 13	12 7	6	5	4	3	2	1	0
CREG	Z	DST	SCR2	SRC1/CST	OP	1	0	0	0	0	S	P
3		5	5	5	6							

FIG. 3C

LOAD/STORE WITH 15-BIT OFFSET (ON THE .D UNIT)

31 29	28	27 23	22 8	7	6 4	3	2	1	0
CREG	Z	DST/SRC	UCST15	Y	LD/ST	1	1	S	P
3		5	15		3				

FIG. 3D

LOAD/STORE 'BASER' + 'OFFSETR/CST' ON THE .D UNIT

31 29	28	27 23	22 18	17 13	12 9	8	7	6 4	3	2	1	0
CREG	Z	DST/SRC	BASE R	OFFSET R/UCST5	MODE	R	Y	LD/ST	0	1	S	P
3		5	5	5	4			3				

FIG. 3E

OPERATIONS ON THE .S UNIT

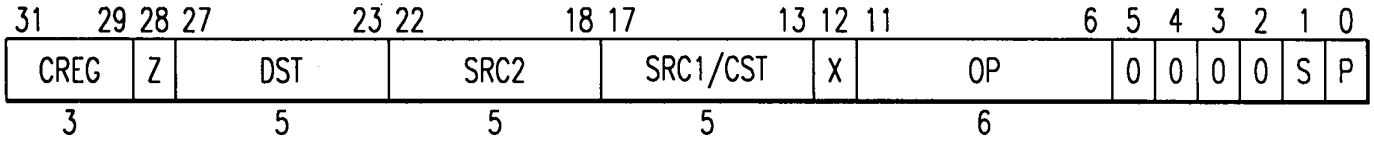


FIG. 3F

ADDK ON THE .S UNIT

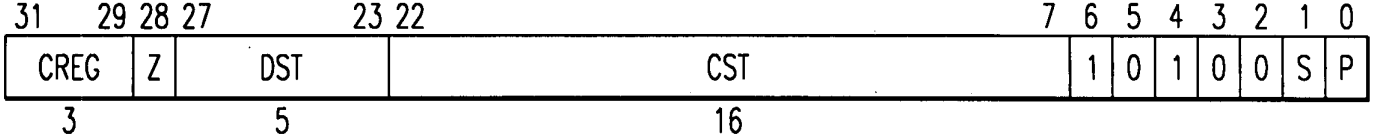


FIG. 3G

BITFIELD OPERATIONS (IMMEDIATE FORMS) ON THE .S UNIT

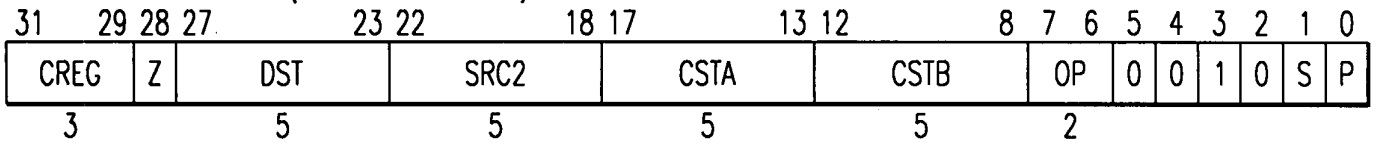


FIG. 3H

MVK AND MVKH ON THE .S UNIT

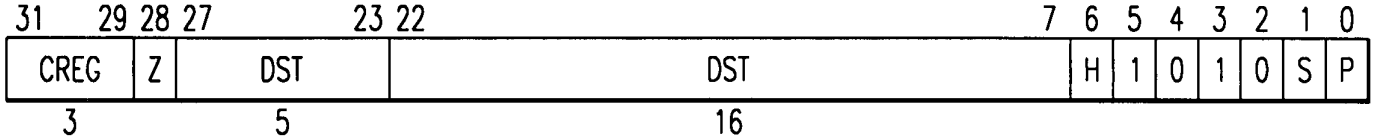


FIG. 3I

BCOND DISP ON THE .S UNIT

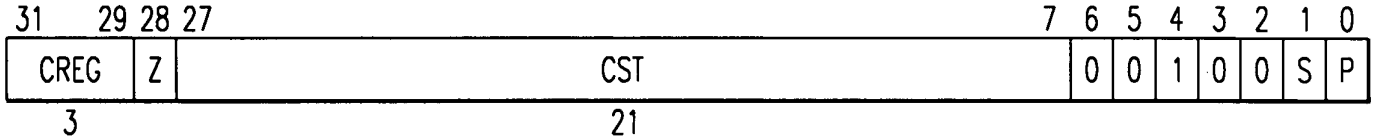


FIG. 3J

FIG. 4

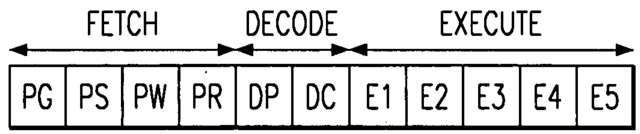


FIG. 5

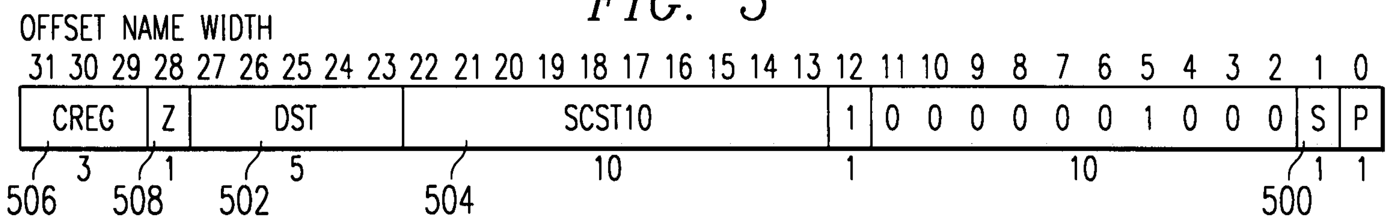


FIG. 6A

PIPELINE STAGE	E1	PS	PW	PR	DP	DC	E1
READ	dst						
WRITTEN	dst, PC						
BRANCH TAKEN							X

FIG. 6B

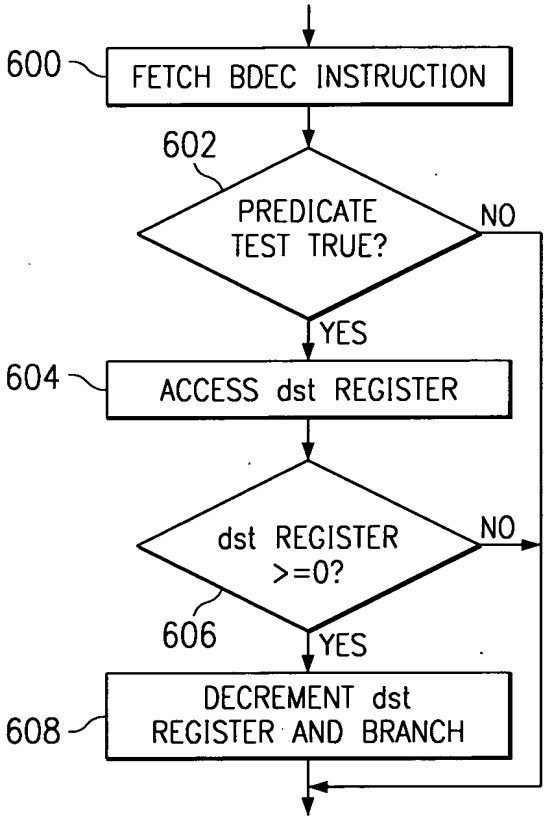


FIG. 9

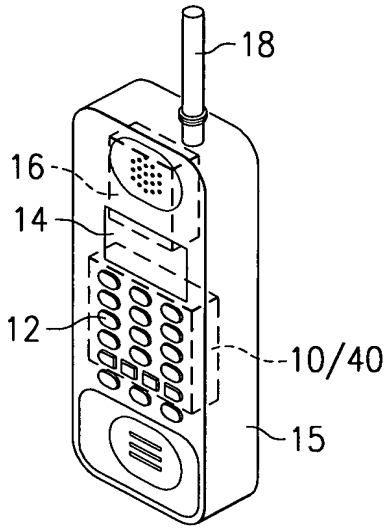
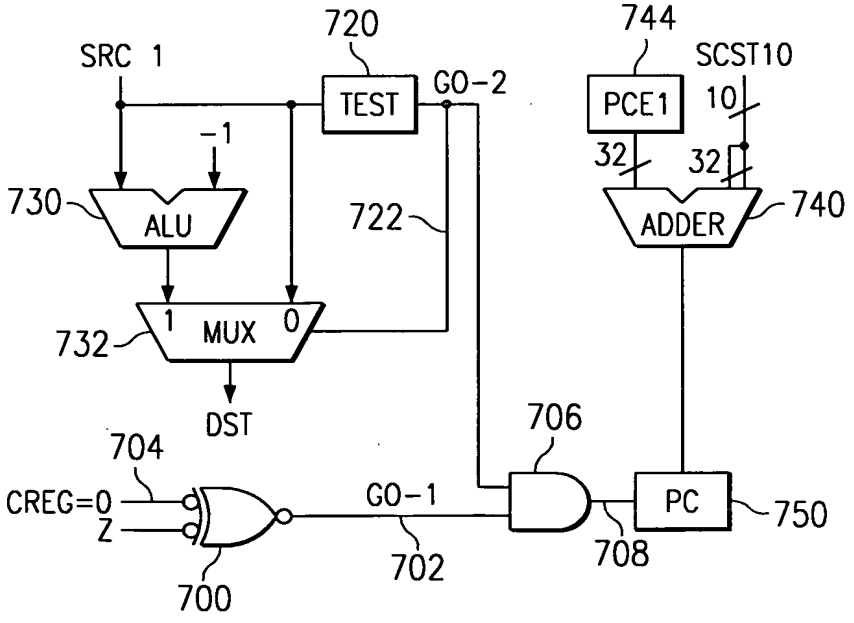


FIG. 7



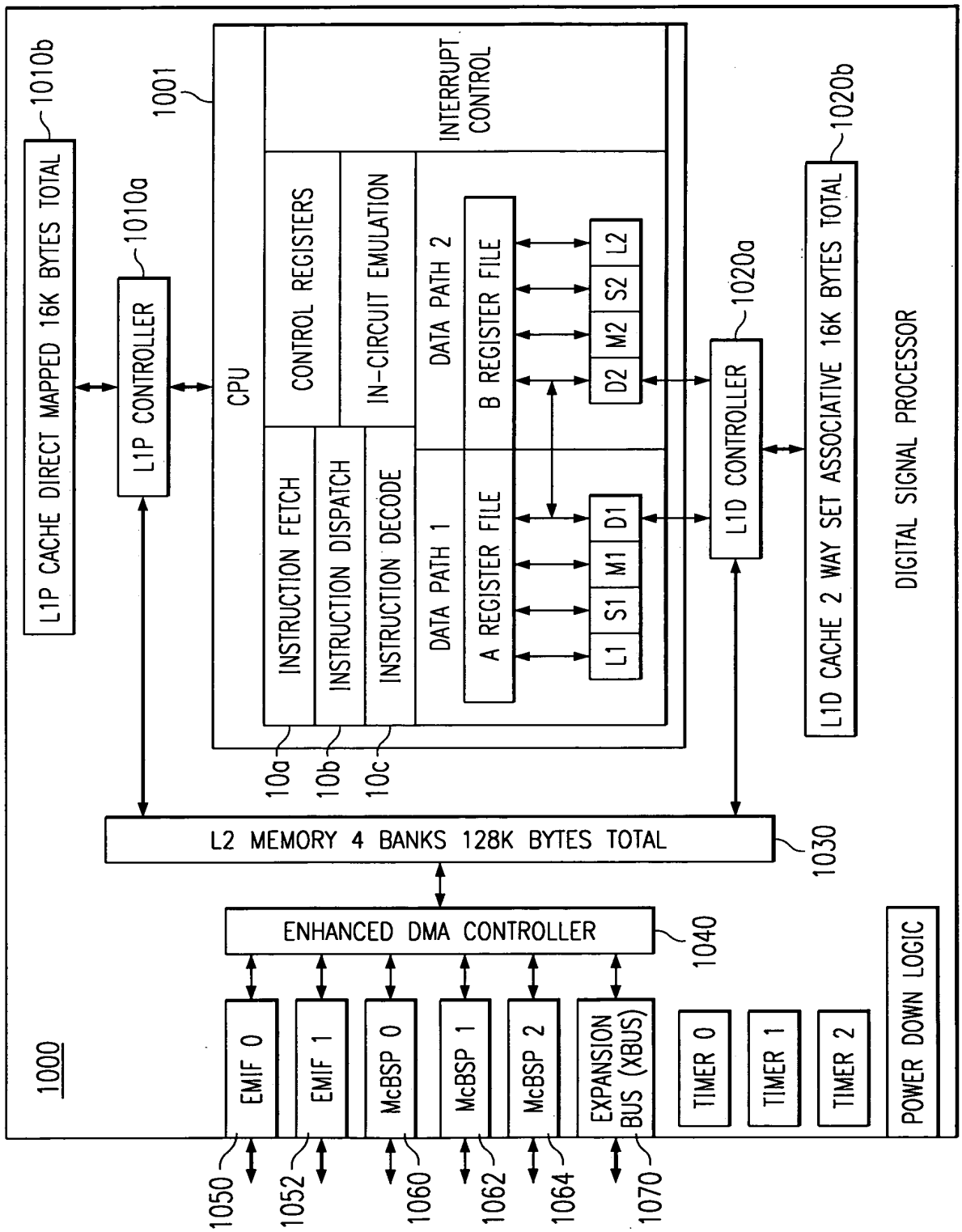

1000
L1P CACHE DIRECT MAPPED 16K BYTES TOTAL
1010b
L1P CONTROLLER
1010a
1001
CPU
INSTRUCTION FETCH
INSTRUCTION DISPATCH
INSTRUCTION DECODE
CONTROL REGISTERS
IN-CIRCUIT EMULATION
INTERRUPT CONTROL
DATA PATH 1
A REGISTER FILE
L1 S1 M1 D1
DATA PATH 2
B REGISTER FILE
D2 M2 S2 L2
10a
10b
10c
L1D CONTROLLER
1020a
L1D CACHE 2 WAY SET ASSOCIATIVE 16K BYTES TOTAL
1020b
DIGITAL SIGNAL PROCESSOR
L2 MEMORY 4 BANKS 128K BYTES TOTAL
1030
ENHANCED DMA CONTROLLER
1040
EMIF 0
EMIF 1
McBSP 0
McBSP 1
McBSP 2
EXPANSION BUS (XBUS)
TIMER 0
TIMER 1
TIMER 2
POWER DOWN LOGIC
1050
1052
1060
1062
1064
1070

FIG. 8